Most Frequently Occurring Classifications of Patents Returned
From A Search of 09/699,589 on June 24, 2003

Combined Classifications

12 438/637
12 438/638
8 438/633
7 257/758
7 438/672
6 257/E21.589
6 438/624
6 438/666
5 438/634
5 438/687
5 438/738
4 257/640
4 257/E21.576
4 257/E21.585
4 257/E23.145
4 438/622
4 438/623
4 438/631
4 438/699
3 257/752
3 257/E21.252
3 257/E21.579
3 438/627
3 438/639
3 438/668
3 438/692
3 438/702
3 438/706
3 438/711
3 438/723
3 438/725
2 148/DIG 100
2 148/DIG 131
2 205/118
2 205/122
2 205/123
2 205/125
2 205/126
2 257/519
2 257/522
2 257/639
2 257/643
2 257/751
2 257/760
2 257/762
2 257/773
2 257/774
2 257/E21.245
2 257/E21.546
2 257/E21.577
2 257/E21.58
2 257/E21.587

2 257/E23.144
2 257/E23.161
2 257/E23.167
2 428/161
2 428/164
2 428/213
2 428/448
2 428/472
2 428/698
2 428/699
2 438/618
2 438/620
2 438/653
2 438/670
2 438/691
2 438/694
2 438/695
2 438/703
2 438/740
2 438/783
2 438/924

12 438/637 (2 OR, 10 XR)
Class 438 : SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS

438/584 COATING WITH ELECTRICALLY OR THERMALLY CONDUCTIVE MATERIAL
438/597 .To form ohmic contact to semiconductive material
438/618 ..Contacting multiple semiconductive regions (i.e., interconnects)
438/622 ...Multiple metal levels, separated by insulating layer (i.e., multiple level metallization)
438/637 ....With formation of opening (i.e., viahole) in insulative layer

12 438/638 (8 OR, 4 XR)
Class 438 : SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS

438/584 COATING WITH ELECTRICALLY OR THERMALLY CONDUCTIVE MATERIAL
438/597 .To form ohmic contact to semiconductive material
438/618 ..Contacting multiple semiconductive regions (i.e., interconnects)
438/622 ...Multiple metal levels, separated by insulating layer (i.e., multiple level metallization)
438/637 ....With formation of opening (i.e., viahole) in insulative layer
438/638 .....Having viaholes of diverse width

8 438/633 (4 OR, 4 XR)
Class 438 : SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS

438/584 COATING WITH ELECTRICALLY OR THERMALLY CONDUCTIVE MATERIAL
438/597 .To form ohmic contact to semiconductive material
438/618 ..Contacting multiple semiconductive regions (i.e., interconnects)
438/622 ...Multiple metal levels, separated by insulating layer (i.e., multiple level metallization)
438/631 ....Having planarization step
438/633 .....Simultaneously by chemical and mechanical means

7 257/758 (3 OR, 4 XR)
Class 257 : ACTIVE SOLID-STATE DEVICES
257/734 COMBINED WITH ELECTRICAL CONTACT OR LEAD
257/741 .Of specified material other than unalloyed aluminum
257/750 ..Layered
257/758 ...Multiple metal levels on semiconductor, separated by insulating layer (e.g., multiple level metallization for integrated circuit)

7 438/672 (0 OR, 7 XR)
Class 438 : SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS

438/584 COATING WITH ELECTRICALLY OR THERMALLY CONDUCTIVE MATERIAL
438/597 .To form ohmic contact to semiconductive material
438/669 ..And patterning of conductive layer
438/672 ...Plug formation (i.e., in viahole)

6 257/E21.589 (0 OR, 6 XR)
Class 257 : ACTIVE SOLID-STATE DEVICES
257/E21.531 ...For electrical parameters, e.g., resistance, deep-levels, CV, diffusions by electrical means (EPO)
257/E21.532 .Manufacture or treatment of devices consisting of plurality of solid state components formed in or on common substrate or of parts thereof; manufacture of integrated circuit devices or of parts thereof (EPO)
257/E21.536 ..Manufacture of specific parts of devices (EPO)
257/E21.575 ...Interconnections, comprising conductors and dielectrics, for carrying current between separate components within device (EPO)
257/E21.576 ....Characterized by formation and post-treatment of dielectrics, e.g., planarizing (EPO)
257/E21.589 .....By forming conductive members before deposition of protective insulating material, e.g., pillars, studs (EPO)

6 438/624 (3 OR, 3 XR)
Class 438 : SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS

438/584 COATING WITH ELECTRICALLY OR THERMALLY CONDUCTIVE MATERIAL
438/597 .To form ohmic contact to semiconductive material
438/618 ..Contacting multiple semiconductive regions (i.e., interconnects)
438/622 ...Multiple metal levels, separated by insulating layer (i.e., multiple level metallization)
438/624 ....Separating insulating layer is laminate or composite of plural insulating materials

6 438/666 (0 OR, 6 XR)
Class 438 : SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS

438/584 COATING WITH ELECTRICALLY OR THERMALLY CONDUCTIVE MATERIAL
438/597 .To form ohmic contact to semiconductive material
438/666 ..Specified configuration of electrode or contact

5 438/634 (1 OR, 4 XR)
Class 438 : SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS

438/584 COATING WITH ELECTRICALLY OR THERMALLY

CONDUCTIVE MATERIAL
438/597 .To form ohmic contact to semiconductive material
438/618 ..Contacting multiple semiconductive regions (i.e., interconnects)
438/622 ...Multiple metal levels, separated by insulating layer (i.e., multiple level metallization)
438/631 ....Having planarization step
438/634 .....Utilizing etch-stop layer

5 438/687 (1 OR, 4 XR)
Class 438 : SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS

438/584 COATING WITH ELECTRICALLY OR THERMALLY CONDUCTIVE MATERIAL
438/597 .To form ohmic contact to semiconductive material
438/687 ..Copper of copper alloy conductor

5 438/738 (0 OR, 5 XR)
Class 438 : SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS

438/689 CHEMICAL ETCHING
438/706 .Vapor phase etching (i.e., dry etching)
438/735 ..Differential etching of semiconductor substrate
438/737 ...Substrate possessing multiple layers
438/738 ....Selectively etching substrate possessing multiple layers of differing etch characteristics

4 257/640 (0 OR, 4 XR)
Class 257 : ACTIVE SOLID-STATE DEVICES
257/629 WITH MEANS TO CONTROL SURFACE EFFECTS
257/632 .Insulating coating
257/635 ..Multiple layers
257/640 ...At least one layer of silicon nitride

4 257/E21.576 (0 OR, 4 XR)
Class 257 : ACTIVE SOLID-STATE DEVICES
257/E21.531 ...For electrical parameters, e.g., resistance, deep-levels, CV, diffusions by electrical means (EPO)
257/E21.532 .Manufacture or treatment of devices consisting of plurality of solid state components formed in or on common substrate or of parts thereof; manufacture of integrated circuit devices or of parts thereof (EPO)
257/E21.536 ..Manufacture of specific parts of devices (EPO)
257/E21.575 ...Interconnections, comprising conductors and dielectrics, for carrying current between separate components within device (EPO)
257/E21.576 ....Characterized by formation and post-treatment of dielectrics, e.g., planarizing (EPO)

4 257/E21.585 (0 OR, 4 XR)
Class 257 : ACTIVE SOLID-STATE DEVICES

PLUS Search Results for S/N 09/699,589, Searched June 24, 2003 (Top 50)

6153935	5960318	6362093	6429119	4470874
4430365	6004883	6365505	6429523	6097092
5208170	6133144	6372631	6440838	6171971
5371047	6165898	6372635	6440863	6221229
5723381	6174804	6380078	6444573	6221229
5948701	6181012	6383919	6518671	4541169
4549927	6287961	6391766	4962058	4541168
5189506	6326300	6399486	5539255	4600624
5328553	6350649	6399496	5663101	4601939
5654216	6358797	6429116	5960254	4799990